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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,177	01/19/2006	Naoki Ando	SONYJP33397	9285

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EXAMINER	
CHAN, EMILY Y	
ART UNIT	PAPER NUMBER
2829	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,177	ANDO, NAOKI	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *4-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/19/2006;3/16/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-3 in the reply filed on 4/02/2007 is acknowledged.

Claim withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claims 4-6, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/02/07.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims 2-3 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 4 and 8 of U.S. Patent No. 7,009,418 in view of Kaneko et al (JP 2000-047255). The claims 2-3 of the

instant invention and the claims 4 and 8 of U.S. Patent No. 7,009,418 are directed to the same display apparatus. The claimed components associated with the functions in the claims 2-3 of the instant invention such as "a semiconductor substrate" and "driver means" are all recited in the claims 4 and 8 of U.S. Patent No. 7,009,418. The only difference between the claims 2-3 of the instant invention and the claims 4 and 8 of U.S. Patent No. 7,009,418 is that the logical operation means recited in the claims 2-3 of the instant invention is not recited in the claims 4 and 8 of U.S. Patent No. 7,009,418; however, the logical operation circuitry in a liquid crystal display panel was old as shown by Kaneko et al ('255) . Kaneko et al ('255) disclose a display (see Figs) and exclusively teach a logical operation means (20). Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the logical operating means (20) as taught by Kaneko et al ('255) into the display apparatus of the claims 4 and 8 of U.S. Patent No. 7,009,418 to make the claims 2-3 of the instant invention comprising the logical operation means because Kaneko et al ('255) disclose that their apparatus operates for checking pixel defect in a state of an array substrate in a short time (see PROBLEM TO BE SOLVED).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaneko et al (JP 2000-047255) in view of Jenkins et al (U S patent No. 6,437,596)

Kaneko et al ('255) expressly disclose a display (see Figs) and a test method for a semiconductor substrate (11) as claimed, comprising:

a semiconductor substrate, a counter substrate and a liquid crystal layer and an image display area (11) in which pixel cell drive circuits each including a pixel switch and a pixel capacitor that is coupled to the pixel switch and holds pixel data are arranged in a matrix corresponding to intersections between data lines and pixel switch control lines;

driver means (17,18) for applying a test drive signal that has a level corresponding to a required logical value to the data lines and gate lines according to operation expression of logical operation executed by logical operation means;

logical operation means (20) for performing the logical operation in accordance with operation expression determined according to the layout structure and/or test item (see MEANS, paragraph [0023]).

Kaneko et al ('255) fail to disclose that their driver means (17,18) operates for applying the test drive signal to each of two or more of the data lines and the two or more data lines being are selected according to an interconnect layout structure on the semiconductor substrate.

Jenkins et al ('596) disclose a display and a test method for a semiconductor substrate (see Figs. 1a-1b) comprising an image display area and a driver means (data line select/hold circuitry 19). Jenkins et al ('596) exclusively teach that their driver means (data line select/hold circuitry 19) operates for applying the test drive signal to two or more of the data lines (see Col. 3, lines 25-30 "for selectively coupling to one or more data lines").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the teaching of Jenkins et al ('596) into Kaneko et al ('255) 's display apparatus for the expected benefit of providing a flexible interface between the array under test and the test system, as disclosed by Jenkins et al ('596) (see Abstract, last four lines).

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tomita (US Patent No. 6,275,061) discloses testing method for a substrate of active matrix display panel (see Fig. 1) comprising data line and gate driving circuits.

Tomita (US Patent No. 7,023,234) discloses a testing method for array substrate (see Fig. 3) comprising a test signal discriminator circuit.

Orii et al (US patent No. 7,009,418) disclose an inspecting method for testing a semiconductor substrate (see Fig. 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha T Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
6/5/07

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER